

FIG. 1

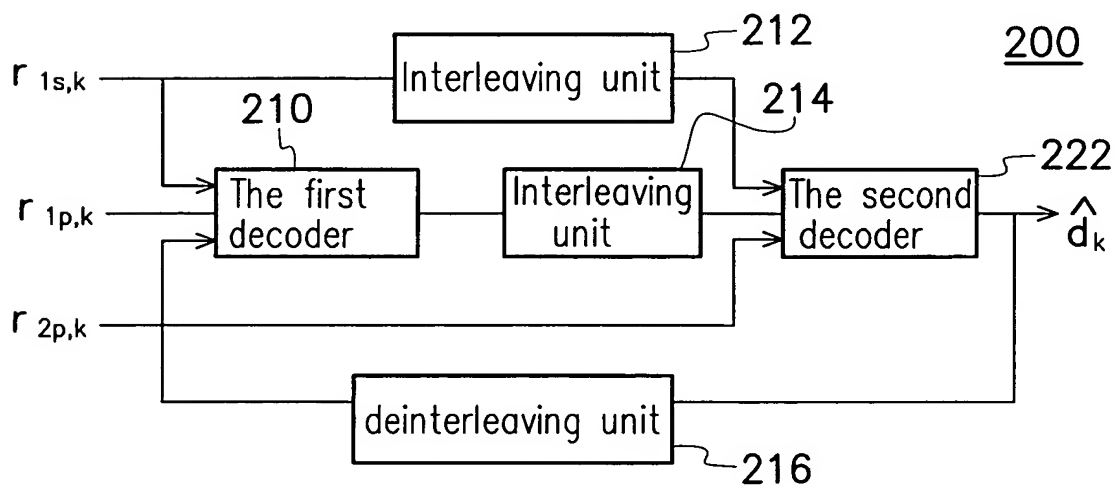


FIG. 2

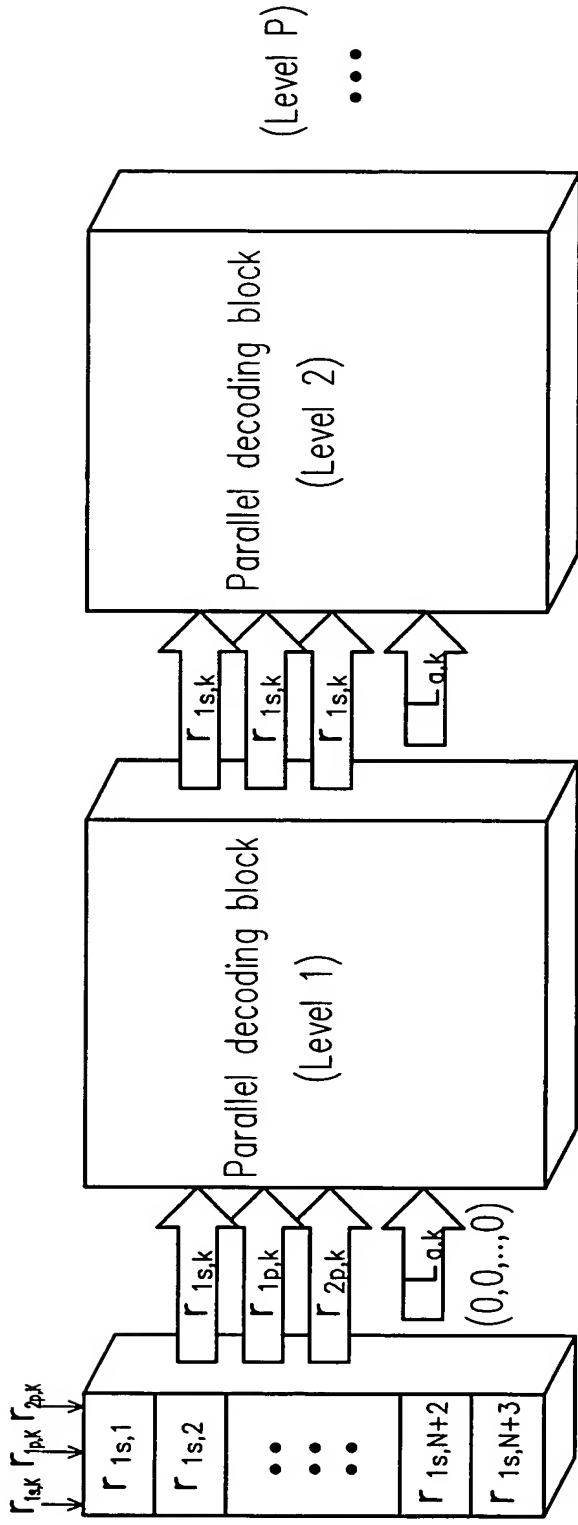


FIG. 3

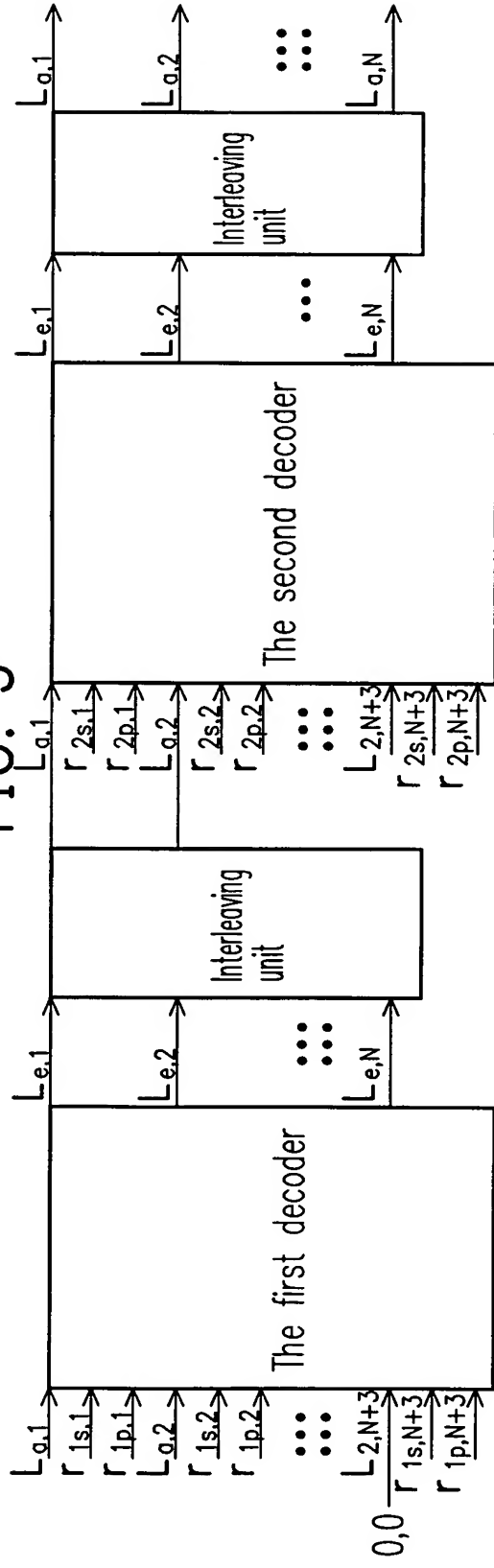
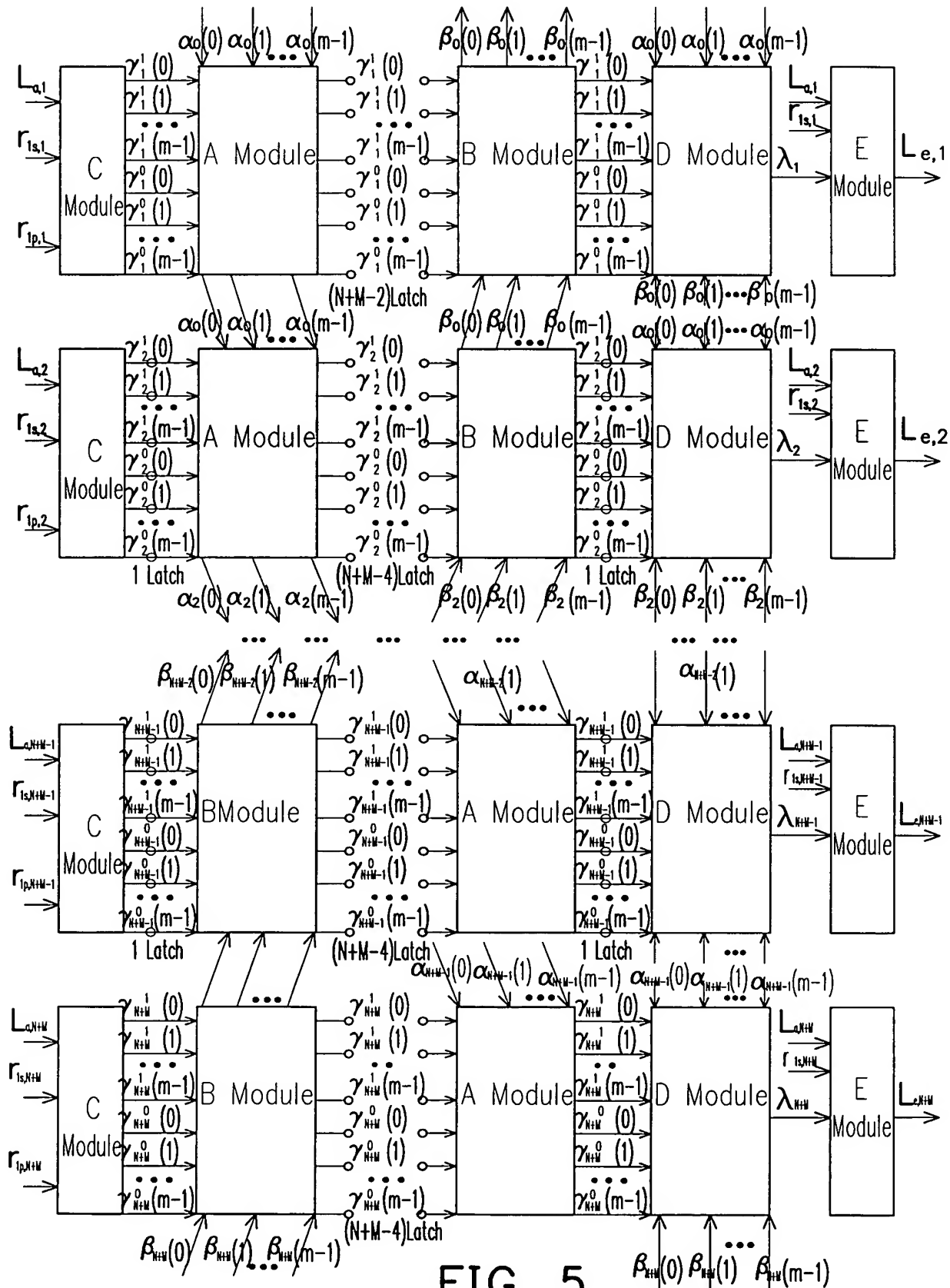


FIG. 4

FIG. 5 is a block diagram of a multi-stage system. The system consists of four stages, each containing a C Module, an A Module, a B Module, a D Module, and an E Module. The C Module receives inputs $L_{a,i}$, $r_{is,i}$, and $r_{ip,i}$ and outputs $\gamma_i^1(0)$ through $\gamma_i^1(m-1)$ and $\gamma_i^0(0)$ through $\gamma_i^0(m-1)$. The A Module receives $\alpha_i(0)$ through $\alpha_i(m-1)$ and $\gamma_i^1(0)$ through $\gamma_i^1(m-1)$ and outputs $\gamma_i^1(0)$ through $\gamma_i^1(m-1)$ and $\gamma_i^0(0)$ through $\gamma_i^0(m-1)$. The B Module receives $\beta_i(0)$ through $\beta_i(m-1)$ and $\gamma_i^1(0)$ through $\gamma_i^1(m-1)$ and outputs $\gamma_i^1(0)$ through $\gamma_i^1(m-1)$ and $\gamma_i^0(0)$ through $\gamma_i^0(m-1)$. The D Module receives $\alpha_i(0)$ through $\alpha_i(m-1)$ and $\gamma_i^1(0)$ through $\gamma_i^1(m-1)$ and outputs $\gamma_i^1(0)$ through $\gamma_i^1(m-1)$ and $\gamma_i^0(0)$ through $\gamma_i^0(m-1)$. The E Module receives λ_i and outputs $L_{e,i}$. The system is controlled by a sequence of latches: $(N+M-2)$ Latch, $(N+M-4)$ Latch, $(N+M-4)$ Latch, and $(N+M-4)$ Latch. The diagram also shows a sequence of inputs $\alpha_i(0)$ through $\alpha_i(m-1)$ and $\beta_i(0)$ through $\beta_i(m-1)$ for each stage i .



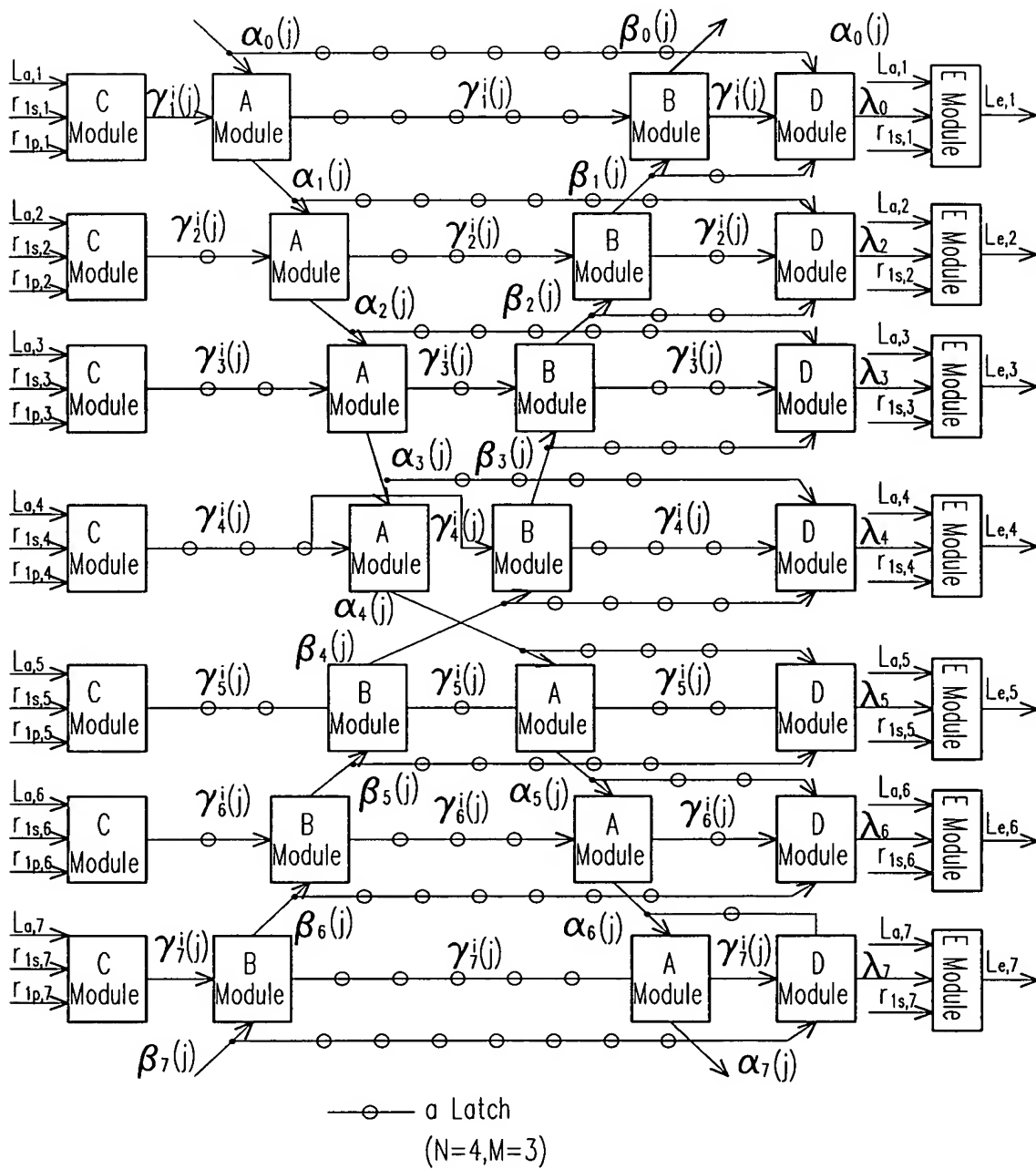


FIG. 6

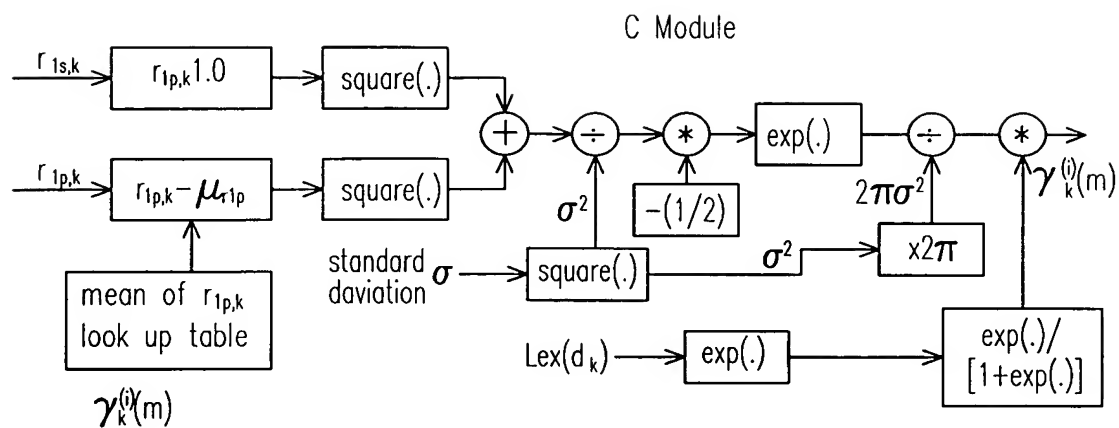


FIG. 7

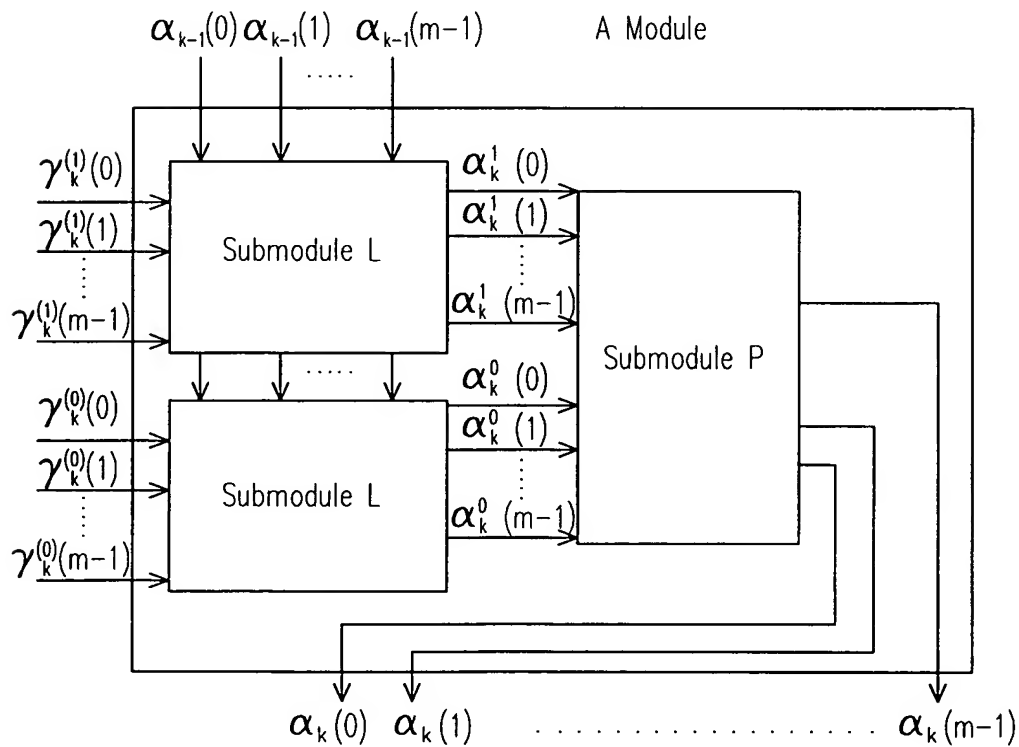


FIG. 8

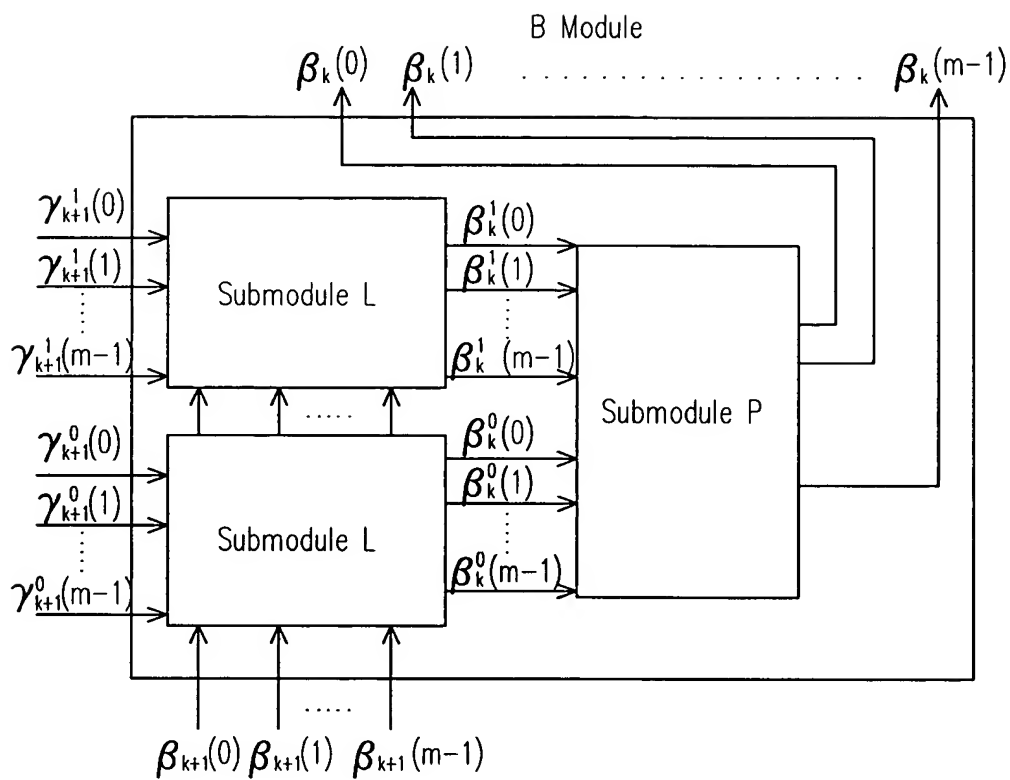


FIG. 9

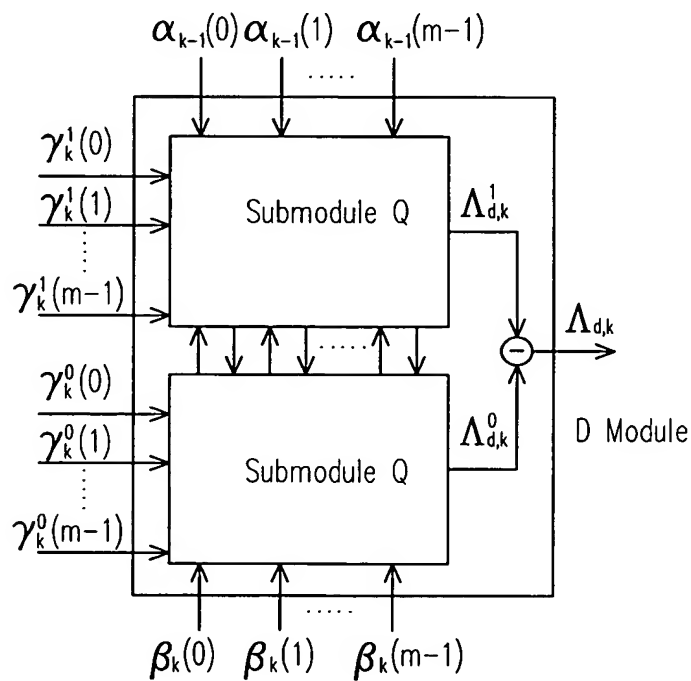


FIG. 10

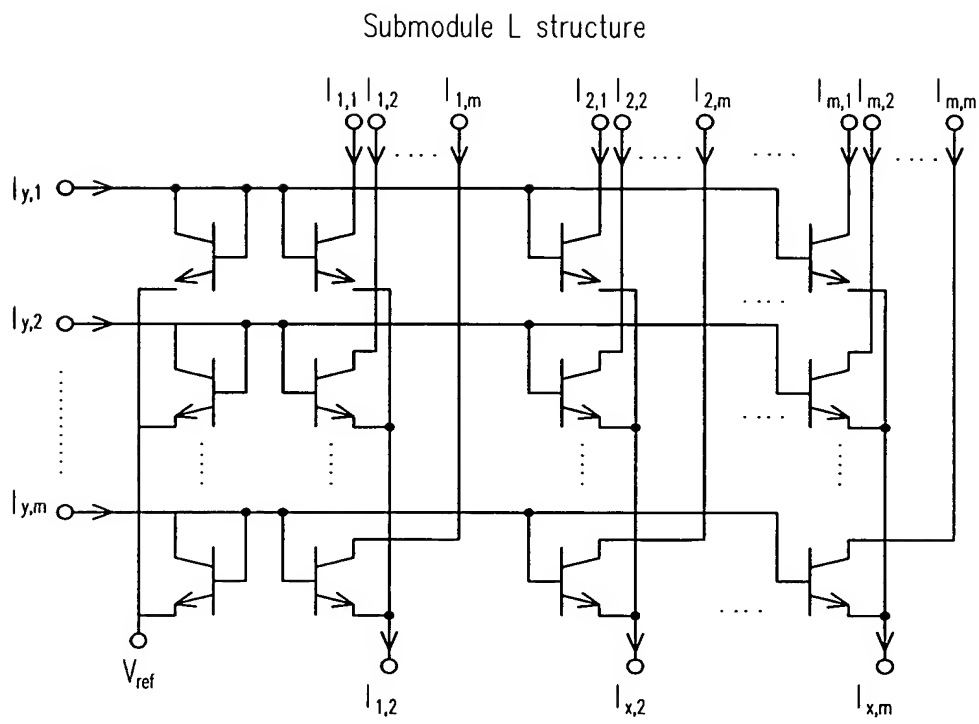


FIG. 11

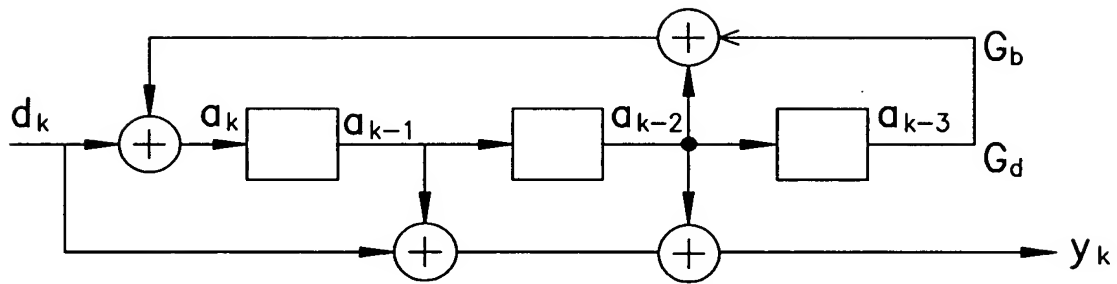


FIG. 12

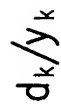


FIG. 13

FIG. 14 is a block diagram of a digital signal processor (DSP) architecture. The architecture includes a multiplier (Mu) and a bypass (A) block. The multiplier (Mu) is used to calculate the product of two inputs, A and B, resulting in C (C=A*B). The bypass (A) block provides a direct path for input A. The DSP architecture is divided into two main sections: Submodule L and Submodule P. Submodule L contains a series of multiplier blocks (Mu) and bypass blocks (A) that process inputs $\alpha_k(0)$ through $\alpha_k(7)$ and $\gamma_k^{(0)}(0)$ through $\gamma_k^{(0)}(7)$. Submodule P contains a series of multiplier blocks (Mu) and bypass blocks (A) that process inputs $\alpha_k(0)$ through $\alpha_k(7)$ and $\gamma_k^{(0)}(0)$ through $\gamma_k^{(0)}(7)$. The outputs of Submodule L and Submodule P are combined in a final multiplier block (Mu) to produce the final output C.

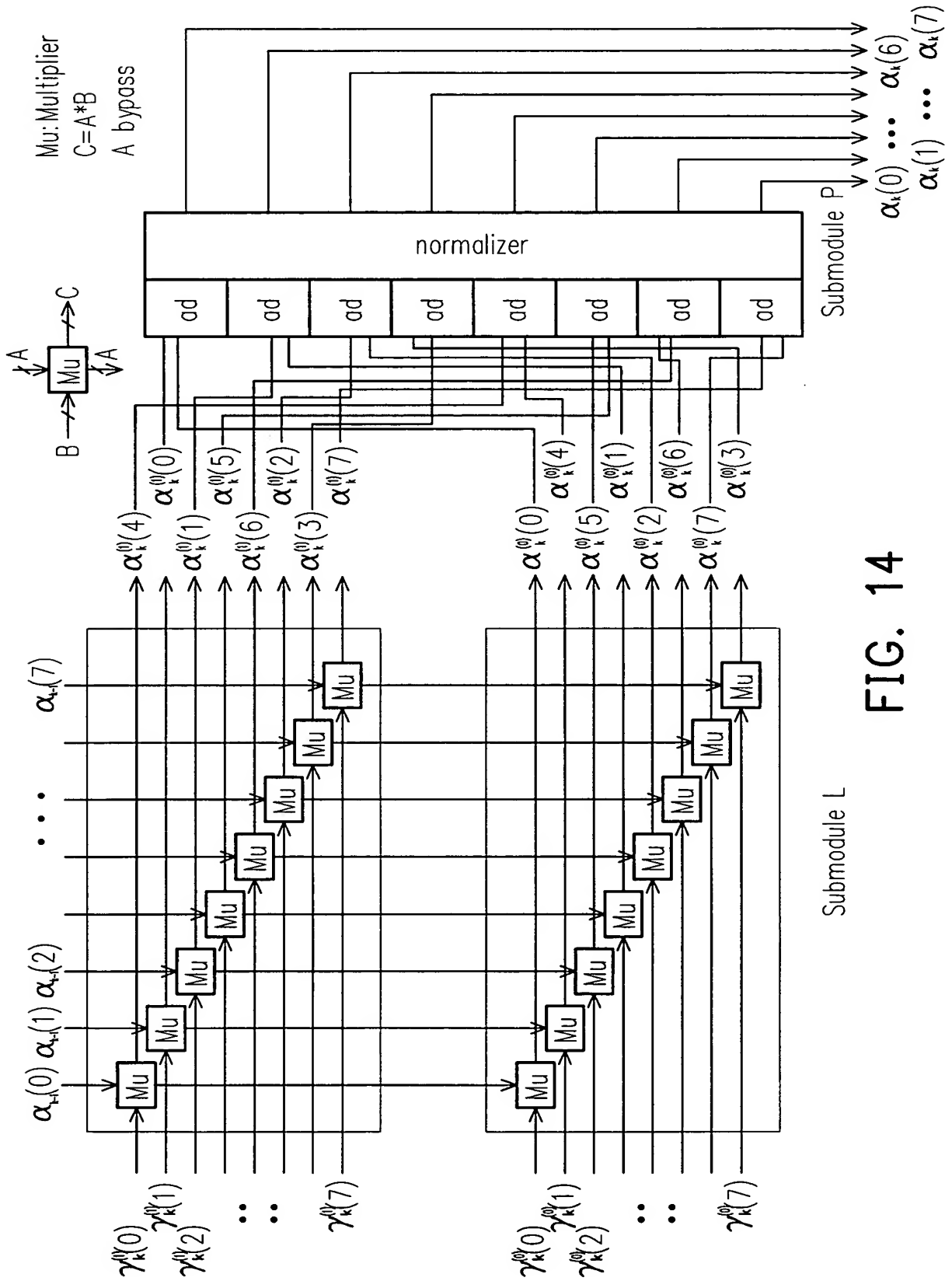


FIG. 14

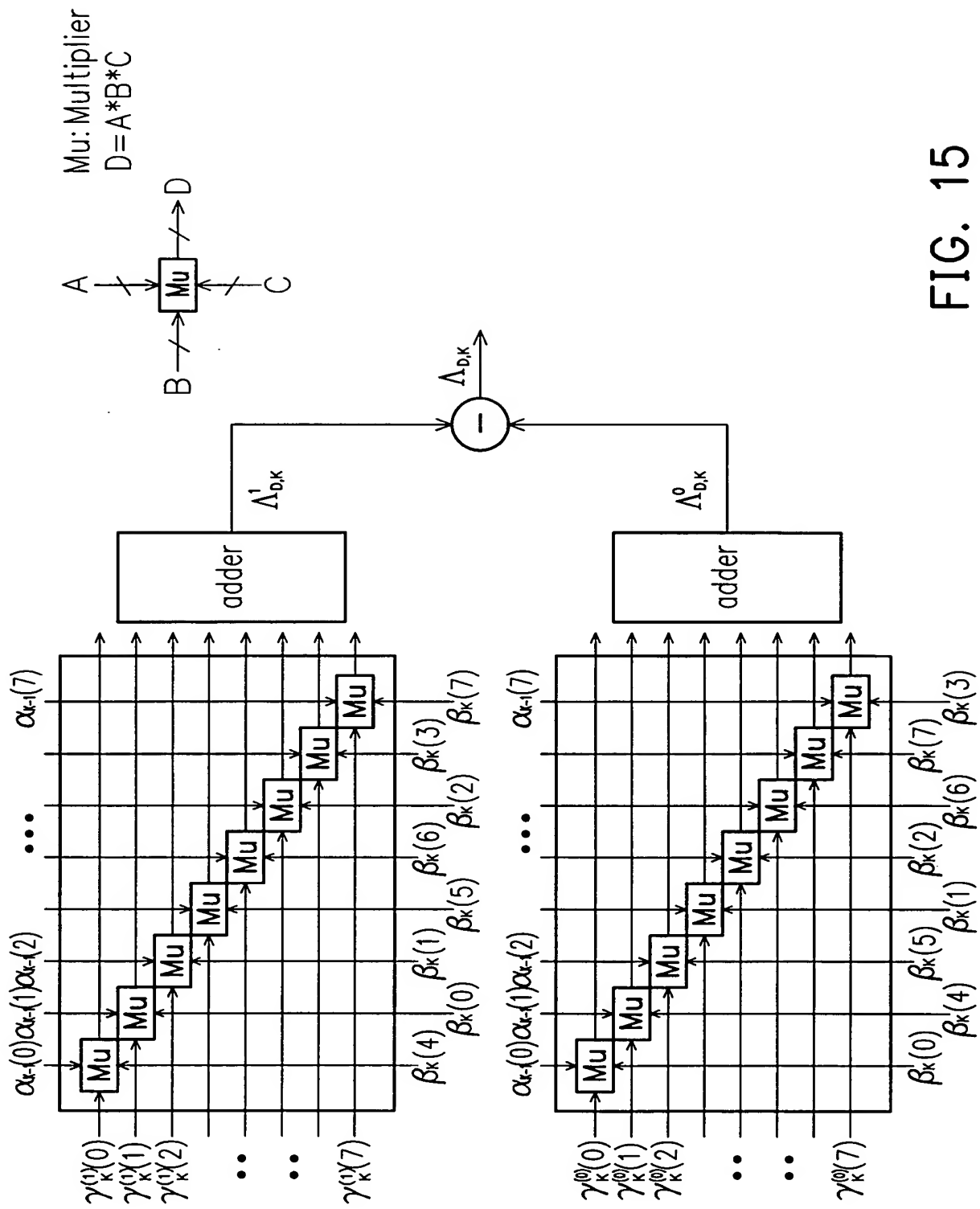


FIG. 15

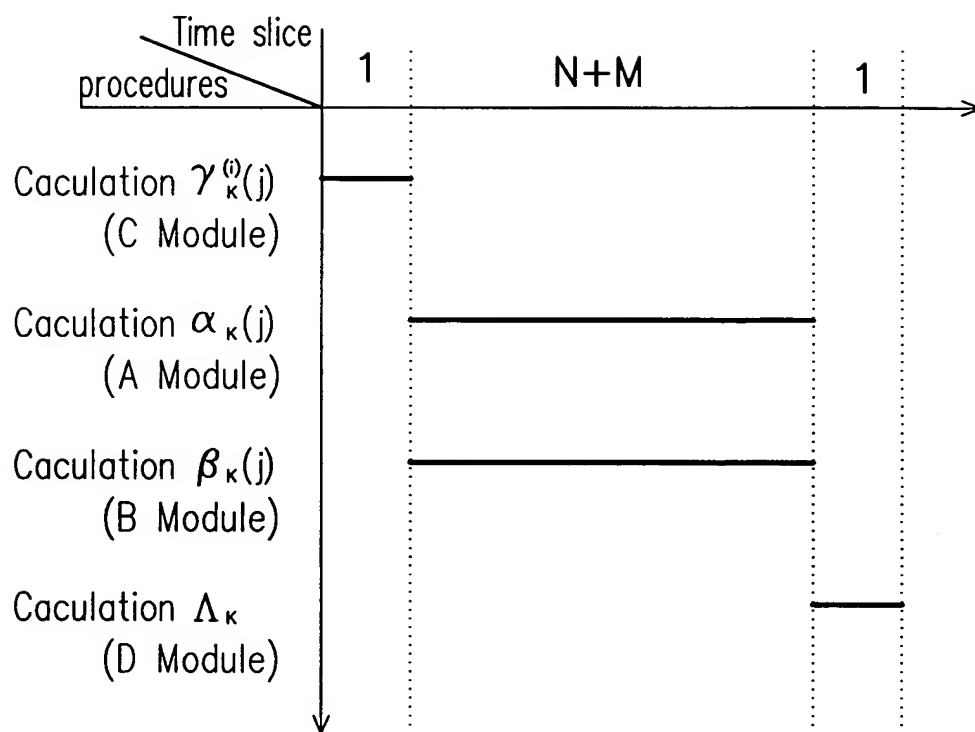


FIG. 16

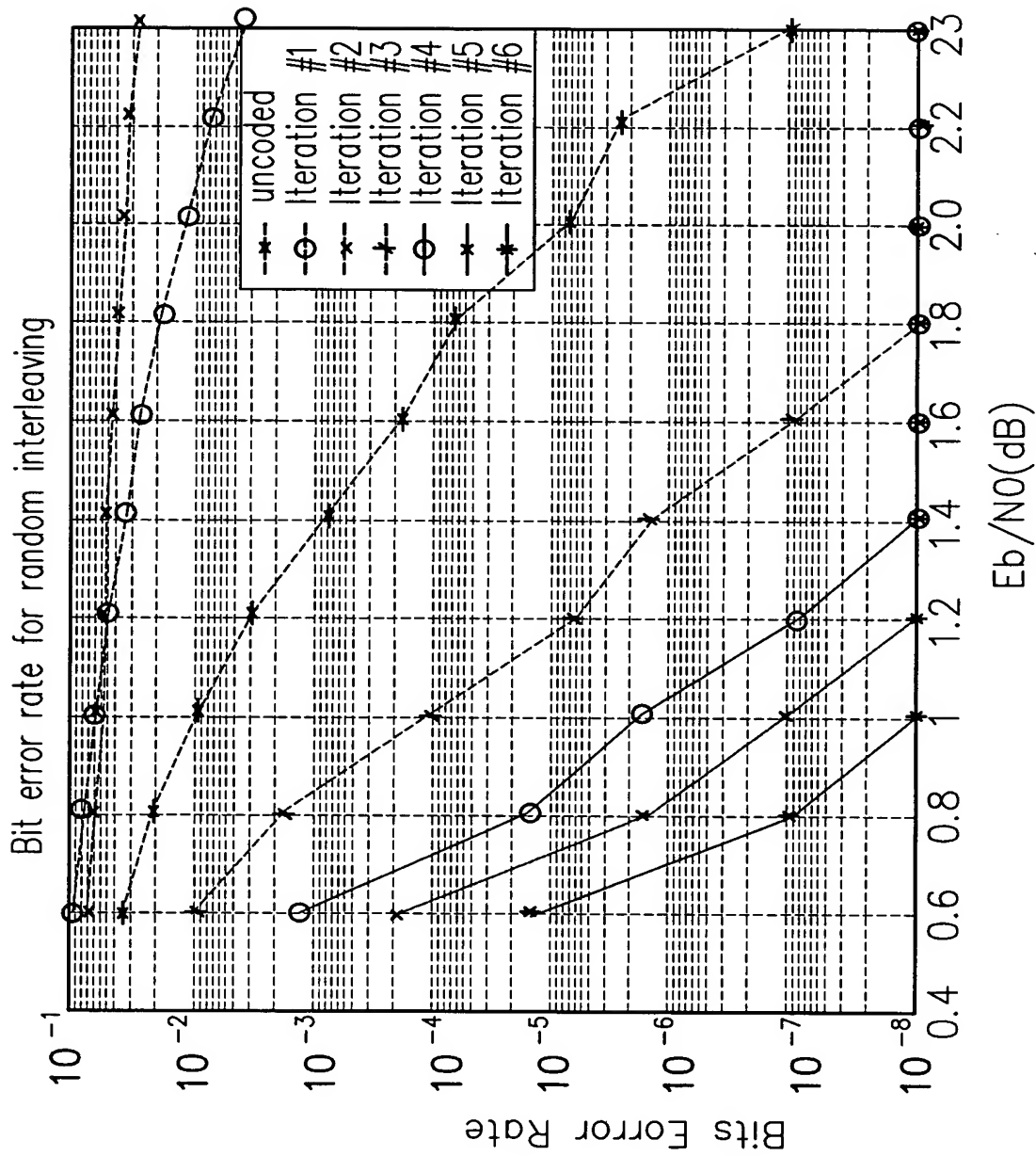


FIG. 17